In the Specification:

Please amend paragraph [0005] beginning on page 2 as follows:

[0005] A layered structure such as a membrane is a common structure in fabricating many semiconductor devices and systems. For example, a silicon or polysilicon membrane parallel to the wafer may be used as an optical mirror. In adaptive optics, such a membrane may be engaged to microactuators to deform in a controlled manner to correct distortions in the wavefront of received optical images. This layered structure may be "natively" grown by directly forming the layer on the wafer on which the final device is fabricated. Alternatively, it may be advantageous or necessary to fabricate such a layer on a separate substrate and then transfer the layer onto ~~over~~ the wafer on which the final device is fabricated.

Please amend paragraph [0006] beginning on page 2 as follows:

[0006] This application includes techniques for transferring a membrane from one wafer to another wafer to form integrated semiconductor devices. According to one embodiment, a carrier wafer is ~~to be~~ fabricated to include a membrane on one side of the carrier wafer. The membrane on the carrier wafer is

then bond to a surface of a different, device wafer by a plurality of joints. The joints and the device wafer are then isolated from exposure to etching chemicals. Next, the carrier wafer is selectively etched away to expose the membrane and to leave said membrane on the device wafer.

Please amend paragraph [0018] beginning on page 6 as follows:

[0018] Referring to FIG. 1A, the carrier wafer 100 is a silicon-on-insulator (SOI) wafer which includes the silicon membrane 101 (e.g. on the order of one micron to tens of microns), a thick single-crystal silicon layer 105 (e.g., a few hundred microns), and a thin insulator layer 103 of less than one micron formed of an insulating material such as a silicon oxide and a silicon nitride and sandwiched between the silicon layers 101 and 105. The insulator layer 103 is assumed to be silicon dioxide as an example in the following description. A semiconductor other than silicon may be used for the wafers 100 and 200, including germanium, a III-V compound like GaAs and GaP, and a II-VI compound. The use of GaAs and other semiconductors for semiconductor opto-electronic devices as the device wafer 200 allows for integration opto-electronic components in the final device.

Please amend paragraph [0024] beginning on page 10 as follows:

[0024] Next, the remaining peripheral region 302 of the wafer 200 is removed by a reactive ion etching process. This may be achieved by using a shadow mask 400 to block the exposed membrane 101 and applying the SF6 plasma to selectively etch the region 302 **(FIG. 4A)**. The shadow mask 400 may also be designed to pattern the transferred membrane 101. FIG. 4B shows the final structure with the membrane 101 integrated on the device wafer 200.

Please amend paragraph [0032] beginning on page 14 as follows:

[0032] The above wafer-level transfer of a membrane has a number of advantages. For example, the transfer can be designed to avoid the use of adhesives or polymers (i.e. wax, epoxy, or photoresist) for bonding the membrane to the device wafer. This can ~~eliminates~~ **eliminate** residues or cracks and maintain a clean mirror membrane. Also, a continuous membrane with a usable area up to the size of the carrier wafer can be transferred in its entirety. Transfer of a 1-micron thick silicon membrane with a diameter of 100 mm has been

demonstrated. This availability of a large, continuous membrane may be particularly useful in various applications including adaptive optics where discontinuities can ~~to~~ lead to phase errors and other adverse effects.